REMARKS

The claims are claims 1 to 18.

The ABSTRACT has been amended to conform to the current length and content guidelines.

The application has been amended at many locations to correct minor errors and to present uniform language throughout. The amendments include correction of those errors noted by the Examiner.

Claims 1, 2, 10 and 11 are amended to clarify subject matter and distinguish over the references.

Claims 1 and 10 were rejected under 35 U.S.C. 102(a) as anticipated by Shiell et al., U.S. Patent Number 5,961,632.

Claims 1 and 10 recite subject matter not taught in Shiell et al. Claim 1 recites "an instruction fetch unit for simultaneously fetching from memory a group of a plurality of instructions, each such group forming a fetch packet." In a similar fashion, claim 10 recites "simultaneously fetching from a memory a group of a plurality of instructions, each such group forming a fetch packet." The OFFICE ACTION fails to point out any portion of Shiell et al disclosing the simultaneous fetching of such fetch packets. Shiell et al fails to state that simultaneously fetched instructions form the recited fetch packet. Accordingly, claims 1 and 10 are allowable over Shiell et al.

Claims 1 and 10 recite subject further matter not taught in Shiell et al. Claims 1 and 10 each recite "the fetch packet having an operating mode in dependence upon the execution mode at the time the request was made to the memory for the fetch packet." The OFFICE ACTION fails to point out any portion of Shiell et al disclosing the selection of operating mode based upon the claimed fetch packets. Shiell et al teaches at column 4, line 27 to column 6, line 37 and illustrated in Figures 2a and 2b that mode is

dependent upon an instruction leading code. This differs from the current mode when the fetch packet is fetched form memory. Accordingly, claims 1 and 10 are allowable over Shiell et al.

Claim 1 recites further subject matter not anticipated by Shiell et al. Claim 1 recites "a shared datapath by both the base and migrant architectures for parsing said base architecture mode and migrant architecture mode fetch packets into execute packets." Shiell et al fails to disclose such a shared data path. Note that Figures 1, 3a and 3b of Shiell et al show direct connection between instruction fetch stage 12 and demultiplexer 14. Thus Shiell et al teaches splitting instructions into separate paths before parsing into execute packets as recited in claim 1. Accordingly, claim 1 is allowable over Shiell et al.

Claims 2 and 11 were rejected under 35 U.S.C 103(a) as made obvious by the combination of Shiell et al., U.S. Patent Number 5,961,632, and Nishioka et al., U.S. Patent Number 6,401,190.

Claims 2 and 11 recite subject matter not made obvious by the combination of Shiell et al and Nishioka et al. Claim 2 recites "a third input to said multiplexer wherein said third input is a no operation machine word." Similarly, claim 11 recites "choosing between the output of said migrant architecture decode and the output of said base architecture decode input and a no operation machine word." Respective base claims 1 and 10 make clear that the machine words result from decoding of individual instructions in the base mode or migrant mode. Nishioka et al fails to disclose these machine words. The nop fields illustrated in Figures 5 and 6 of Nishioka et al are instructions within the original or expanded execute packet and not the no operation machine word claimed. Note that Nishioka et al fails to disclose the decoding of instructions into machine words as claimed. Figure 1 of Nishioka et al shows supply of instruction words stored in instruction registers 14 to 21 to respective computing units 23 to 25. Presumably the decode

of instructions into machine words takes place within computing units 23 to 25 of Nishioka et al. The OFFICE ACTION fails to point out where Nishioka et al discloses or makes obvious the multiplexer selecting between three machine words recited in claim 2 or the selection from three machine words recited in claim 11. Thus, even if the nop instructions of Nishioka et al were the no operation machine word recited in claims 2 and 11, the combination of Shiell et al and Nishioka et al fail to make obvious the selection among three machine words recited in claims 2 and 11. Accordingly, claims 2 and 11 are allowable over the combination of Shiell et al and Nishioka et al.

Claims 1, 2, 10 and 11 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Hammond et al., U.S. Patent Number 5,638,525, and Nishioka et al., U.S. Patent Number 6,401,190.

Claims 1 and 10 recite subject matter not taught in the combination of Hammond et al and Nishioka et al. Claim 1 recites "an instruction fetch unit for simultaneously fetching from memory a group of a plurality of instructions, each such group forming a fetch packet." In a similar fashion, claim 10 recites "simultaneously fetching from a memory a group of a plurality of instructions, each such group forming a fetch packet." The OFFICE ACTION fails to point out any portion of Hammond et al or Nishioka et al disclosing the simultaneous fetching of such fetch packets. Hammond et al discloses fetching individual instructions from instruction cache 320 to demultiplexer 321 "at the appropriate time for decoding" at column 12, lines 7 to 10. Nishioka et al likewise fails to disclose simultaneous fetching of a group of instructions comprising a fetch packet. Accordingly, claims 1 and 10 are allowable over Shiell et al.

Claims 1 and 10 recite subject further matter not taught in the combination of Hammond et al and Nishioka et al. Claims 1 and

10 each recite "the fetch packet having an operating mode in dependence upon the execution mode at the time the request was made to the memory for the fetch packet." The OFFICE ACTION fails to point out any portion of Hammond et al disclosing the selection of operating mode based upon the claimed fetch packets. Hammond et al teaches at column 12, lines 10 to line 27 that the mode is determined for individual instructions and not for the fetch packet as claimed. Nishioka et al add no teaching to Hammond et al to make this subject matter obvious. Accordingly, claims 1 and 10 are allowable over the combination of Hammond et al and Nishioka et al.

Claim 1 recites further subject matter not anticipated by the combination of Hammond et al and Nishioka et al. Claim 1 recites "a shared datapath by both the base and migrant architectures for parsing said base architecture mode and migrant architecture mode fetch packets into execute packets." Hammond et al fails to disclose such a shared data path. Note that Figure 3 of Hammond et al shows a direct connection between instruction cache 320 and demultiplexer 321. Thus Hammond et al teaches splitting instructions into separate paths before parsing into execute packets as recited in claim 1. Accordingly, claim 1 is allowable over the combination of Hammond et al and Nishioka et al.

Claims 2 and 11 recite subject matter not made obvious by the combination of Hammond et al and Nishioka et al. Claim 2 recites "a third input to said multiplexer wherein said third input is a no operation machine word." Similarly, claim 11 recites "choosing between the output of said migrant architecture decode and the output of said base architecture decode input and a no operation machine word." Respective base claims 1 and 10 make clear that the machine words result from decoding of individual instructions in the base mode or migrant mode. Hammond et al fails to disclose these machine words. The nop fields illustrated in Figures 5 and 6 of Nishioka et al are instructions within the original or expanded

execute packet and not the no operation machine word claimed. Note that Nishioka et al fails to disclose the decoding of instructions into machine words as claimed. Figure 1 of Nishioka et al shows supply of instruction words stored in instruction registers 14 to 21 to respective computing units 23 to 25. Presumably the decode of instructions into machine words takes place within computing units 23 to 25 of Nishioka et al. The OFFICE ACTION fails to point out where Nishioka et al discloses or makes obvious the multiplexer selecting between three machine words recited in claim 2 or the selection from three machine words recited in claim 11. Neither the portions of Nishioka et al cited in the OFFICE ACTION nor Figures 5 or 6 teach the claimed multiplexer. Thus, even if the nop instructions of Nishioka et al were the no operation machine word recited in claims 2 and 11, the combination of Hammond et al and Nishioka et al fail to make obvious the selection among three machine words recited in claims 2 and 11. Accordingly, claims 2 and 11 are allowable over the combination of Hammond et al and Nishioka et al.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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